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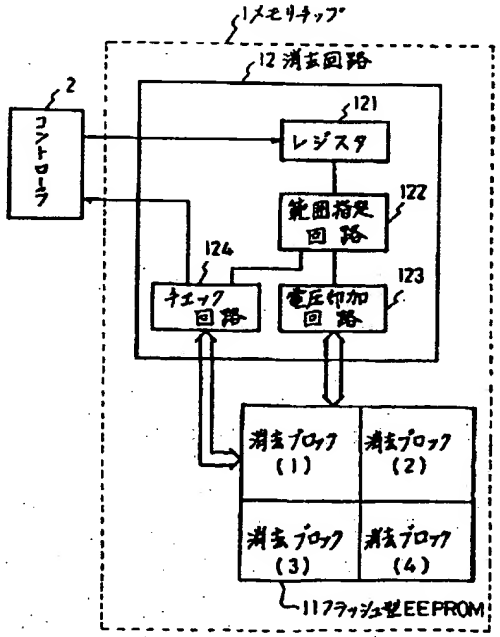
(54)【発明の名称】　半導体ファイル装置

(57)【要約】

【目的】　本発明は、複数の消去ブロックの消去を短時間に行うことができると共に、前記消去にかかる消費電力を低減させることができる半導体ファイル装置を提供することを目的としている。

【構成】　本発明において、消去回路１２の範囲指定回路１２２は、コントローラ２によりレジスタ１２１に設定された複数の消去ブロックに対する消去指令に基づいて消去する範囲を求め、これを電圧印加回路１２３に与える。電圧印加回路１２３はフラッシュ型ＥＥＰＲＯＭ１１内の前記与えられた消去範囲に一度に電圧をかけて前記範囲内の複数の消去ブロックを一度に消去する。



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【特許請求の範囲】

【請求項1】　フラッシュ型ＥＥＰＲＯＭにデータを読み書きする半導体ファイル装置において、前記フラッシュ型ＥＥＰＲＯＭ内に割り付けられた複数の任意に指定された消去ブロックに消去電圧を一度にかけて前記複数の消去ブロックを一度に消去する消去手段を具備したことを特徴とする半導体ファイル装置。

【請求項2】　前記任意に指定された複数の消去ブロックが複数のメモリチップに亙ることを特徴とする請求項1記載の半導体ファイル装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はフラッシュ型ＥＥＰＲＯＭにデータを読み書きする半導体ファイル装置に係わり、特に前記ＥＥＰＲＯＭ内のデータの消去に関する。

【0002】

【従来の技術】従来、フラッシュ型ＥＥＰＲＯＭは特定のメモリ領域を一度に消去することができ、前記特定のメモリ領域を消去ブロックと称する。このようなフラッシュ型ＥＥＰＲＯＭを用いた半導体ファイル装置は例えば図２に示すような構成を有している。コントローラ２はメモリチップ１内のフラッシュ型ＥＥＰＲＯＭ１１にデータの書き込みを行う前に、このフラッシュ型ＥＥＰＲＯＭ１１の例えば消去ブロック（１）～（３）を消去する動作を行う。即ち、コントローラ２はメモリチップ１内のフラッシュ型ＥＥＰＲＯＭ１１内の消去ブロック（１）を消去する指令を出す。これにより、消去回路１２は消去ブロック（１）に消去電圧をかけて消去する。次にコントローラ２はフラッシュ型ＥＥＰＲＯＭ１１内の消去ブロック（２）を消去する指令を出す。これにより、消去回路１２は消去ブロック（２）に消去電圧をかけて消去する。更にコントローラ２はフラッシュ型ＥＥＰＲＯＭ１１内の消去ブロック（３）を消去する指令を出す。これにより、消去回路１２は消去ブロック（３）に消去電圧をかけて消去する。従って、上記のように複数の消去ブロックを消去する場合、消去ブロック（１）、（２）、（３）の順番で逐次消去が行われる。或いはコントローラ２が前記消去回路１２に全消去ブロックの消去を指令すると、消去回路１２は消去ブロック（１）～（４）の全てを一度に消去する。

【0003】従って、上記従来の半導体ファイル装置では、複数の消去ブロックのデータを書き替える前に、前記ブロックの消去を逐次行うため、消去時間が長くなると共に、消去のための消費電力が余計にかかるという欠点があった。尚、消去回路１２により消去ブロックを消去する際に必要とする消去電圧は昇圧回路（図示せず）にて昇圧して作るが、この昇圧に電力を要するため、ブロック消去を行うごとに電力を喰うことになる。しかも、消去ブロックの消去自体には消去電圧をかけるだけで余り電力を必要としないため、同一面積の領域を一度

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で消去した場合と、複数回に亙って消去した場合では、複数回に渡って消去した場合の方が余計に電力を喰うことになる。

【0004】

【発明が解決しようとする課題】フラッシュ型ＥＥＰＲＯＭを用いる従来の半導体ファイル装置では、前記フラッシュ型ＥＥＰＲＯＭにデータを書き込む前に、前記フラッシュ型ＥＥＰＲＯＭの前記データが書かれる消去ブロックを事前に消去しなければならないが、この消去は逐次行われるため、消去に時間がかかると共に、消去にかかる消費電力が大きくなってしまうという欠点があった。

【0005】そこで本発明は上記の欠点を除去し、複数の消去ブロックの消去を短時間に行うことができると共に、前記消去にかかる消費電力を低減させることができる半導体ファイル装置を提供することを目的としている。

【0006】

【課題を解決するための手段】本発明はフラッシュ型ＥＥＰＲＯＭにデータを読み書きする半導体ファイル装置において、前記フラッシュ型ＥＥＰＲＯＭ内に割り付けられた複数の任意に指定された消去ブロックに消去電圧を一度にかけて前記複数の消去ブロックを一度に消去する消去手段を具備した構成を有する。

【0007】

【作用】本発明のフラッシュ型ＥＥＰＲＯＭにおいて、消去手段はフラッシュ型ＥＥＰＲＯＭ内に割り付けられた複数の任意に指定された消去ブロックに消去電圧を一度にかけて、前記複数の消去ブロックを一度に消去する。

【0008】

【実施例】以下、本発明の一実施例を図面を参照して説明する。図１は本発明の半導体ファイル装置の一実施例を示したブロック図である。１はメモリチップで、２のコントローラと共に半導体ファイル装置を構成している。メモリチップ１にはフラッシュ型ＥＥＰＲＯＭ１１と消去回路１２が内蔵されている。消去回路１２は消去ブロック情報などを保持するレジスタ１２１、フラッシュ型ＥＥＰＲＯＭ１１内の消去範囲を電圧印加回路１２３に指定する範囲指定回路１２２、フラッシュ型ＥＥＰＲＯＭ１１の消去範囲に消去電圧を印加してデータの消去を行う電圧印加回路１２３及び消去が正常に行われたか否かをチェックするチェック回路１２４を有している。又、フラッシュ型ＥＥＰＲＯＭ１１には消去ブロック（１）～（４）が割り付けられている。尚、消去電圧は図示されない昇圧回路から電圧印加回路１２３に供給されるものとする。

【0009】次に本実施例の動作について説明する。コントローラ２は例えば消去ブロック（１）、（２）、（３）にデータを書き込む前に、これら消去ブロックを

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消去する動作を行う。即ち、コントローラ２は消去回路１２のレジスタ１２１に消去ブロック（1）、（2）、（3）を消去する指令を設定して、これら指令を保持させる。範囲指定回路１２２はレジスタ１２１に設定されている消去対象消去ブロックに基づいて、今回一度に消去するフラッシュ型ＥＥＰＲＯＭ１１の消去範囲を求め、この消去範囲（ここでは消去ブロック（1）～（3））を電圧印加回路１２３及びチェック回路１２４に与える。電圧印加回路１２３は与えられた範囲、即ち、この例では消去ブロック（1）～（3）の範囲に消去電圧を一度にかけて、これら消去ブロック（1）～（3）内のデータを一度に消去する。チェック回路１２４は今し方消去された消去ブロック内をチェックして、消去が完全に行われたことを確認すると、これをコントローラ２に知らせる。コントローラ２は消去が完全に行われたことを知ると、前記消去ブロック（1）～（3）へのデータの書き込み動作に移行する。尚、チェック回路１２４により消去が行われていない部分が見つかった場合、コントローラ２は前記部分を含む消去ブロックの消去指令を消去回路１２に再度出して、前記消去ブロックの消去を上記と同様に行う。

【００１０】次に上記コントローラ２が複数のメモリチップ１を制御する構成のものでは、複数のメモリチップ１に亙る複数の消去ブロックを一度に消去しなければならないことが生じるが、このような場合の動作は以下に述べる如くである。即ち、コントローラ２は消去したい消去ブロックを有するメモリチップ１の各消去回路１２のレジスタ１２１に、該当する消去ブロックの消去指令を設定する。その後、各メモリチップ１の消去回路１２内の電圧印加回路１２３が、前記レジスタ１２１内の情報に基づいて範囲指定回路１２２より求められたフラッシュ型ＥＥＰＲＯＭ１１の消去範囲に、消去電圧を一斉

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に同期してかければ、複数のメモリチップ１に亙る複数の消去ブロックが一度に消去される。

【００１１】本実施例によれば、メモリチップ１の消去回路１２はコントローラ２から指定された複数のフラッシュ型ＥＥＰＲＯＭ１１内の消去ブロックに一度に消去電圧をかけることにより、前記複数の消去ブロックを一度に消去することができる。このため、従来の如く複数の消去ブロックを逐次消去することがなくなり、複数の消去ブロックの消去時間を短縮化することができると共に、消去で消費される電力を低減することができる。又、消去時間を短縮化できるため、データの書き込みを高速化することができる。更に、複数のメモリチップ１に亙る複数の消去ブロックに対しても同様の方法で一度に消去でき、同様の効果がある。

【００１２】

【発明の効果】以上記述した如く本発明の半導体ファイル装置によれば、複数の消去ブロックの消去を短時間に行うことができると共に、前記消去にかかる消費電力を低減させることができる。

【図面の簡単な説明】

【図１】本発明の半導体ファイル装置の一実施例を示したブロック図。

【図２】従来の半導体ファイル装置の一例を示したブロック図。

【符号の説明】

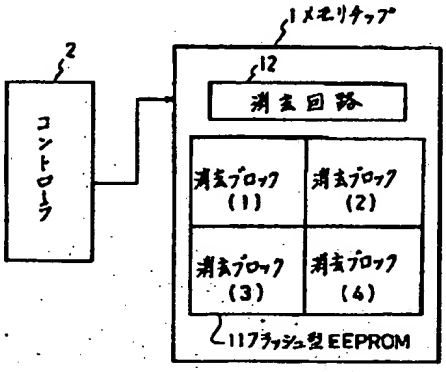
１…メモリチップ　２…コントローラ

１１…フラッシュ型ＥＥＰＲＯＭ　１２…消去回路

１２１…レジスタ　１２２…範囲指定回路

１２３…電圧印加回路　１２４…チェック回路

【図２】



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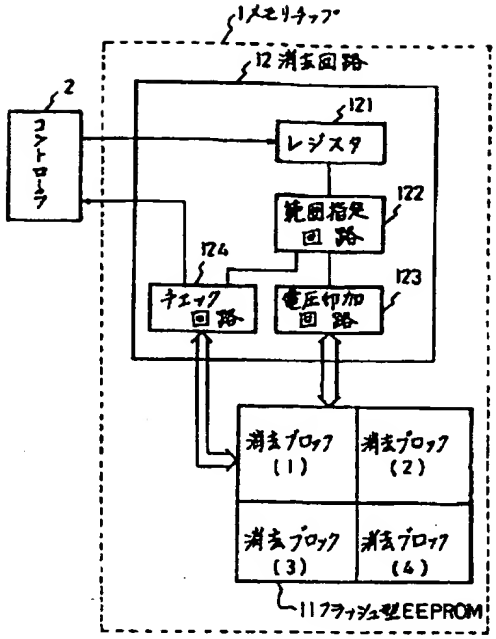
【図1】


1メモリチップ
12 消去回路
2
コントローラ
121
レジスタ
122
範囲指定回路
124
チェック回路
123
電圧印加回路
消去ブロック(1)
消去ブロック(2)
消去ブロック(3)
消去ブロック(4)
11 フラッシュ型EEPROM

FH 008613

Japanese Patent Laid-Open No. 131889/1994

Laid-Open Date: May 13, 1994

Application Date: October 14, 1992

Applicant: Toshiba Corporation

Title:

SEMICONDUCTOR FILING DEVICE

Abstract:

[Purpose] To provide a semiconductor filing device capable of erasing a plurality of erasure blocks in a short time and reducing consumption power required for the above erasing.

[Constitution] According to the invention, a range specifying circuit 122 of an erasing circuit 12 obtains the range to be erased according to an erase command to a plurality of erasure blocks preset in a register 121, and gives the same to a voltage applying circuit 123. The voltage applying circuit 123 applies voltage to the entire given erase range in a flash EEPROM 11 all at once to erase the plurality of erasure blocks in the range all at the same time.

Claims:

1. A semiconductor filing device for reading and writing data to a flash EEPROM, comprising: erasing means for applying erasing voltage to a plurality of arbitrarily specified erasure blocks allocated in the flash EEPROM all at the same time to thereby erase the plurality of erasure blocks all at the same

time.

2. The semiconductor filing device according to claim 1, wherein the plurality of the arbitrarily specified erasure blocks extend over a plurality of memory chips.

Detailed Description of the Invention:

[0001]

[Industrial Field of Application]

This invention relates to a semiconductor filing device for reading and writing data to a flash EEPROM and particularly to erasing of data in the EEPROM.

[0002]

[Prior Art]

FH 008615

In the conventional flash EEPROM, specified memory areas are erased all at one time, and this specified memory area is called an erasure block. A semiconductor filing device using the flash EEPROM has the configuration shown in Fig. 2, for example. A controller 2 conducts the operation of erasing for example erasure blocks 1 to 3 of the flash EEPROM 11 in a memory chip before writing data 1 to the flash EEPROM 1. The controller 2 gives a command for erasing the erasure block (1) of the flash EEPROM 11 in the memory chip 1. In response to the command, an erasing circuit 12 applies erasing voltage to the erasure block 1 to be erased. Subsequently, the controller 2 gives a command for erasing the erasure block 2 of the flash EEPROM

11. In response to the command, the erasing circuit 12 applies erasing voltage to the erasure block (2) to be erased. Further, the controller 2 gives a command for erasing the erase block 3 of the flash EEPROM 11. In response to the command, the erasing circuit 12 applies erasing voltage to the erasure block (3) to be erased. Accordingly, in the case of erasing the plural erasure blocks as described above, erasing is performed sequentially in the order of (1), (2) and (3). When the controller 2 gives a command for erasing all erasure blocks to the erasing circuit 12, the erasing circuit 12 erases all of the erasure blocks (1) to (4) at the same time.

[0003] **FH 008616**

Consequently, in the conventional semiconductor filing apparatus, before the data of the plural erasure blocks is rewritten, erasing is sequentially performed for the blocks, resulting in the disadvantage that the erase time becomes longer and the extra consumption power for erasing is required. The erasing voltage required for erasing the erasure blocks by the erasing circuit 12 is produced by raising the voltage in a boosting circuit (not shown), so the power is required for raising the voltage so that the power is consumed in every execution of block erasing. Erasing of the erasure block per se does not require much power because only the erasing voltage is applied thereto, so when the case of erasing the region of the same area at the same time is compared with the case of

erasing the same with multiple applications of voltage, the case of erasing the region with multiple applications of voltage consumes much more power.

[0004]

[Problems that the Invention is to Solve]

In the conventional semiconductor filing device using the flash EEPROM, it is necessary to erase the erasure block where data is to be written in the flash EEPROM before writing data in the flash EEPROM, and erasing is sequentially performed, resulting in the disadvantage that it takes much time for erasing, and the consumption power for erasing becomes larger.

[0005]

It is, accordingly, an object of the invention to overcome the above disadvantage and provide a semiconductor filing device capable of erasing a plurality of erasure blocks in a short time and reducing the consumption power for the above erasing.

[0006]

[Means for Solving the Problems]

According to the invention, the semiconductor filing device for reading and writing data to a flash EEPROM includes erasing means for applying erasing voltage to a plurality of arbitrarily specified erasure blocks allocated in the flash EEPROM at the same time to erase the plurality of erasure blocks at the same time.

[0007]

[Operation]

In the flash EEPROM of the invention, the erasing means applies erasing voltage to a plurality of arbitrarily specified erasure blocks at the same time to thereby erase the plurality of erasure blocks at the same time.

[0008]

[Embodiment]

One embodiment of the invention will now be described with reference to the attached drawings. Fig. 1 is a block diagram showing one embodiment of a semiconductor filing device according to the invention. The reference numeral 1 designates a memory chip, which constitutes a semiconductor filing device with a controller designated by the reference numeral 2. In the memory chip 1 is incorporated a flash EEPROM 11 and an erasing circuit 12. The erasing circuit 12 has a register 121 for holding erasure block information, a range specifying circuit 122 for specifying an erase range in the flash EEPROM 11 to a voltage applying circuit 123, a voltage applying circuit 123 for applying erasing voltage to an erase range of the flash EEPROM 11 to erase data, and a check circuit 124 for checking whether erasing has been properly performed or not. The erasure blocks (1) to (4) are allocated in the flash EEPROM 11. The erasing voltage is supplied from a boosting circuit not shown to the voltage applying circuit 123.

[0009]

The operation of the embodiment will now be described. The controller 2 conducts the operation of erasing the erasure blocks (1), (2), (3) before writing data in the erasure blocks. The controller 2 sets commands for erasing the erasure blocks (1), (2), (3) in the register 121 of the erasing circuit 12, which holds the commands. The range specifying circuit 122 receives the erase range of the flash EEPROM 11 which is to be erased at the same time according to the erasure blocks set in the register 121 as the blocks to be erased, and sends the erase range (the erasure blocks (1) to (3) here) to the voltage applying circuit 123 and the checking circuit 124. The voltage applying circuit 123 applies the erasing voltage to the given range, that is, the range of the erasure blocks (1) to (3) in this example at the same time, thereby erasing the data in the erasure blocks (1) to (3) at the same time. The check circuit 124 checks the erasure blocks erased just now, and on confirming the completion of erasing, it reports the completion to the controller 2. The controller 2 causes the transition to the operation of writing the data into the erasure blocks (1) to (3) after it knows erasing has been completed. When it is found by the check circuit 124 that there is a portion not yet erased, the controller 2 again gives an erase command for the erasure block containing the above portion not erased to the erasing circuit 12 to perform erasing of the erasure block, similarly to the above.

[0010]

In the constitution where the controller 2 controls a plurality of memory chips 1, it is sometimes necessary to erase a plurality of erasure blocks extending over the plurality of memory chips 1 at the same time. The operation in that case is as follows. The controller 2 sets an erase command for the concerned erasure blocks in the register of each erasing circuit 12 of the memory chips 1 having the erasure blocks to be erased. After that, when the voltage applying circuit 123 in the erasing circuit 12 of each memory chip 1 applies the erasing voltage to the erasure range of the flash EEPROM 11 obtained from the range specifying circuit 122 according to the information in the register 121 simultaneously, the plurality of erasure blocks extending over a plurality of memory chips are erased at the same time.

FH 008620

[0011]

According to the present embodiment, the erasing circuit 12 of the memory chip 1 can erase the plurality of erasure blocks at the same time by applying erasing voltage to the plurality of erasure blocks in the EEPROM 11 specified by the controller 2 at the same time. Therefore, it is not necessary to sequentially erase the plurality of erasure blocks as before so that the erase time for the plurality of erasure blocks can be reduced and the power consumed in erasing can be reduced. Furthermore, the erase time can be reduced so that high speed

writing of data can be achieved. Further, the plurality of erasure blocks extending over the plurality of memory chips 1 can be erased at the same time by the similar method, so the similar effect can be produced.

[0012]

[Effect of the Invention]

According to the invention, as described above, the semiconductor filing device can erase the plurality of erasure blocks in a short time and reduce the consumption power required for the above erasing.

Brief Description of the Drawings:

Fig. 1 is a block diagram showing one embodiment of a semiconductor filing device according to the invention; and

Fig. 2 is a block diagram showing an example of the conventional filing device.

[Description of the Reference Numerals and Signs]

1: memory chip 2: controller 11: flash EEPROM 12: erasing circuit 121: register 122: range specifying circuit 123: voltage applying circuit 124: check circuit

FIGURE 1:

1: MEMORY CHIP 2: CONTROLLER 11: FLASH EEPROM ERASE BLOCKS (1) to (4) 12: ERASING CIRCUIT 121: REGISTER 122: RANGE SPECIFYING CIRCUIT 123: VOLTAGE APPLYING CIRCUIT 124:

CHECK CIRCUIT

FIGURE 2:

1: MEMORY CHIP 2: CONTROLLER 11: FLASH EEPROM ERASE BLOCKS (1) to (4) 12: ERASING CIRCUIT

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[0002]

[Prior Art]

In the conventional flash EEPROM, specified memory areas are erased all at one time, and this specified memory area is called an erasure block. A semiconductor filing device using the flash EEPROM has the configuration shown in Fig. 2, for example. A controller 2 conducts the operation of erasing for example erasure blocks 1 to 3 of the flash EEPROM 11 in a memory chip before writing data 1 to the flash EEPROM 1. The controller 2 gives a command for erasing the erasure block (1) of the flash EEPROM 11 in the memory chip 1. In response to the command, an erasing circuit 12 applies erasing voltage to the erasure block 1 to be erased. Subsequently, the controller 2 gives a command for erasing the erasure block 2 of the flash EEPROM

11. In response to the command, the erasing circuit 12 applies erasing voltage to the erasure block (2) to be erased. Further, the controller 2 gives a command for erasing the erase block 3 of the flash EEPROM 11. In response to the command, the erasing circuit 12 applies erasing voltage to the erasure block (3) to be erased. Accordingly, in the case of erasing the plural erasure blocks as described above, erasing is performed sequentially in the order of (1), (2) and (3). When the controller 2 gives a command for erasing all erasure blocks to the erasing circuit 12, the erasing circuit 12 erases all of the erasure blocks (1) to (4) at the same time.

[0003]

Consequently, in the conventional semiconductor filing apparatus, before the data of the plural erasure blocks is rewritten, erasing is sequentially performed for the blocks, resulting in the disadvantage that the erase time becomes longer and the extra consumption power for erasing is required. The erasing voltage required for erasing the erasure blocks by the erasing circuit 12 is produced by raising the voltage in a boosting circuit (not shown), so the power is required for raising the voltage so that the power is consumed in every execution of block erasing. Erasing of the erasure block per se does not require much power because only the erasing voltage is applied thereto, so when the case of erasing the region of the same area at the same time is compared with the case of

erasing the same with multiple applications of voltage, the case of erasing the region with multiple applications of voltage consumes much more power.

[0004]

[Problems that the Invention is to Solve]

In the conventional semiconductor filing device using the flash EEPROM, it is necessary to erase the erasure block where data is to be written in the flash EEPROM before writing data in the flash EEPROM, and erasing is sequentially performed, resulting in the disadvantage that it takes much time for erasing, and the consumption power for erasing becomes larger.

[0005]

It is, accordingly, an object of the invention to overcome the above disadvantage and provide a semiconductor filing device capable of erasing a plurality of erasure blocks in a short time and reducing the consumption power for the above erasing.

[0006]

[Means for Solving the Problems]

According to the invention, the semiconductor filing device for reading and writing data to a flash EEPROM includes erasing means for applying erasing voltage to a plurality of arbitrarily specified erasure blocks allocated in the flash EEPROM at the same time to erase the plurality of erasure blocks at the same time.

[0007]

[Operation]

In the flash EEPROM of the invention, the erasing means applies erasing voltage to a plurality of arbitrarily specified erasure blocks at the same time to thereby erase the plurality of erasure blocks at the same time.

[0008]

[Embodiment]

One embodiment of the invention will now be described with reference to the attached drawings. Fig. 1 is a block diagram showing one embodiment of a semiconductor filing device according to the invention. The reference numeral 1 designates a memory chip, which constitutes a semiconductor filing device with a controller designated by the reference numeral 2. In the memory chip 1 is incorporated a flash EEPROM 11 and an erasing circuit 12. The erasing circuit 12 has a register 121 for holding erasure block information, a range specifying circuit 122 for specifying an erase range in the flash EEPROM 11 to a voltage applying circuit 123, a voltage applying circuit 123 for applying erasing voltage to an erase range of the flash EEPROM 11 to erase data, and a check circuit 124 for checking whether erasing has been properly performed or not. The erasure blocks (1) to (4) are allocated in the flash EEPROM 11. The erasing voltage is supplied from a boosting circuit not shown to the voltage applying circuit 123.

[0009]

The operation of the embodiment will now be described. The controller 2 conducts the operation of erasing the erasure blocks (1), (2), (3) before writing data in the erasure blocks. The controller 2 sets commands for erasing the erasure blocks (1), (2), (3) in the register 121 of the erasing circuit 12, which holds the commands. The range specifying circuit 122 receives the erase range of the flash EEPROM 11 which is to be erased at the same time according to the erasure blocks set in the register 121 as the blocks to be erased, and sends the erase range (the erasure blocks (1) to (3) here) to the voltage applying circuit 123 and the checking circuit 124. The voltage applying circuit 123 applies the erasing voltage to the given range, that is, the range of the erasure blocks (1) to (3) in this example at the same time, thereby erasing the data in the erasure blocks(1) to (3) at the same time. The check circuit 124 checks the erasure blocks erased just now, and on confirming the completion of erasing, it reports the completion to the controller 2. The controller 2 causes the transition to the operation of writing the data into the erasure blocks (1) to (3) after it knows erasing has been completed. When it is found by the check circuit 124 that there is a portion not yet erased, the controller 2 again gives an erase command for the erasure block containing the above portion not erased to the erasing circuit 12 to perform erasing of the erasure block, similarly to the above.

[0010]

In the constitution where the controller 2 controls a plurality of memory chips 1, it is sometimes necessary to erase a plurality of erasure blocks extending over the plurality of memory chips 1 at the same time. The operation in that case is as follows. The controller 2 sets an erase command for the concerned erasure blocks in the register of each erasing circuit 12 of the memory chips 1 having the erasure blocks to be erased. After that, when the voltage applying circuit 123 in the erasing circuit 12 of each memory chip 1 applies the erasing voltage to the erasure range of the flash EEPROM 11 obtained from the range specifying circuit 122 according to the information in the register 121 simultaneously, the plurality of erasure blocks extending over a plurality of memory chips are erased at the same time.

[0011]

According to the present embodiment, the erasing circuit 12 of the memory chip 1 can erase the plurality of erasure blocks at the same time by applying erasing voltage to the plurality of erasure blocks in the EEPROM 11 specified by the controller 2 at the same time. Therefore, it is not necessary to sequentially erase the plurality of erasure blocks as before so that the erase time for the plurality of erasure blocks can be reduced and the power consumed in erasing can be reduced. Furthermore, the erase time can be reduced so that high speed

writing of data can be achieved. Further, the plurality of erasure blocks extending over the plurality of memory chips 1 can be erased at the same time by the similar method, so the similar effect can be produced.

[0012]

[Effect of the Invention]

According to the invention, as described above, the semiconductor filing device can erase the plurality of erasure blocks in a short time and reduce the consumption power required for the above erasing.

Brief Description of the Drawings:

Fig. 1 is a block diagram showing one embodiment of a semiconductor filing device according to the invention; and

Fig. 2 is a block diagram showing an example of the conventional filing device.

[Description of the Reference Numerals and Signs]

1: memory chip 2: controller 11: flash EEPROM 12: erasing circuit 121: register 122: range specifying circuit 123: voltage applying circuit 124: check circuit

FIGURE 1:

1: MEMORY CHIP 2: CONTROLLER 11: FLASH EEPROM ERASE BLOCKS (1) to (4) 12: ERASING CIRCUIT 121: REGISTER 122: RANGE SPECIFYING CIRCUIT 123: VOLTAGE APPLYING CIRCUIT 124:

CHECK CIRCUIT

FIGURE 2:

1: MEMORY CHIP 2: CONTROLLER 11: FLASH EEPROM ERASE BLOCKS (1) to (4) 12: ERASING CIRCUIT